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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: CHAUHAN

Appl. No.: 10/710,874

Filed: August 10, 2004

For: Reducing Coupling Effect on Reference Voltages  
When Output Buffers Implemented with Low  
Voltage Transistors Generate High Voltage Output  
Signals



Art Unit: UNASSIGNED

Examiner: UNASSIGNED

Atty. Docket: TI-38154

**INFORMATION DISCLOSURE STATEMENT**

Honorable Commissioner for Patents  
Alexandria, VA 22313-1450

Sir:

Listed below on an attached Form PTO-1449 is information known to applicant(s). A copy of each listed publication and foreign patent is being submitted herewith, along with a concise explanation of information in a foreign language, if any, pursuant to 37 C.F.R. §1.97-1.98.

Applicants respectfully request that the listed information be considered by the Examiner and be made of record in the above-identified application. The Examiner is requested to initial and return it in accordance with MPEP §609.

This statement is not intended to represent that the information cited in the statement is, or is considered to be, material to patentability as defined in §1.56. Applicant reserves the right to establish patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information is not enabling for the teachings purportedly offered.

X This statement qualifies under 37 C.F.R. §1.97, subsection (b) because (check all that apply):

- X (1) It is being filed within 3 months of the application filing date; OR  
— (2) It is being filed within 3 months of entry of a national stage; OR  
X (3) It is being filed before the mail date of the first Office Action on the merits.

— 37 C.F.R. §1.97(c). If this statement is being filed after the latest of: (1) three months beyond the filing date of a national application; (2) three months beyond the date of entry of the national stage as set forth in §1.491 in an international application; or (3) the mailing date of a first Office action on the merits, but before the mailing date of the earlier of a final office action under §1.113 or a notice of allowance under §1.311, then:  
— a certification as specified in §1.97(e) is provided below; or  
— a fee of \$180.00 as set forth in §1.17(p) is authorized below, enclosed, or included with the payment of other papers filed together with this statement.

— 37 C.F.R. §1.97(d). If this statement is being filed after the mailing date of the earlier of a final office action under §1.113 or a notice of allowance under §1.311, but before payment of the issue fee, then:  
A. a certification as specified in §1.97(e) is submitted herewith; and  
B. a petition under 37 C.F.R. §1.97(d) requesting consideration of this statement is submitted herewith; and  
C. a fee of \$130.00 as set forth in §1.17(i)(1) is authorized below, enclosed, or included with the payment of other papers filed together with this statement.

Respectfully submitted,

Date: August 11, 2004

By: Naren Thappeta  
Narendra Reddy Thappeta  
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**Complete if Known**

Application Number	10/710874
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<b>Filing Date</b>	August 10, 2004
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First Named Inventor	Rajat Chauhan
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Group Art Unit	UNASSIGNED
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Examiner Name	UNASSIGNED
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Attorney Docket Number	TI-38154
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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

**Abstract**

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of

2

## U.S. PATENT DOCUMENTS

[illegible]

**FOREIGN PATENT DOCUMENTS**

[illegible]

Examiner Signature	Date Considered
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\*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Unique citation designation number. <sup>2</sup> See attached Kinds of U.S. Patent Documents. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

**Burden Hour Statement:** This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.**

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Substitute for form 1449B/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

**Complete if Known**

Application Number	10/710874
Filing Date	August 10, 2004
First Named Inventor	Rajat Chauhan
Group Art Unit	UNASSIGNED
Examiner Name	UNASSIGNED
Attorney Docket Number	TI-38154

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**OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		HECTOR SANCHEZ, JOSHUA SIEGEL, CARMINE NICOLETTA, JAMES .P AND NISSEN ,JOSE ALVAREZ, "A Versatile 3.3V/2.5V/1.8-V CMOS I/O Driver Bulit in a 0.2-um ,3.5nm Toz , 1.8-V CMOS Technology " in IEEE J. Solid State Circuits Vol 34,pp. 1501-1511,No.11, November 1999.	
		CHANGSIK YOO, MIN -KYU KIM , AND WONCHAN KIM , " A Static Power Saving TTL-to -CMOS Input buffer " in IEEE Journal of Solid State Circuits. Vol 30, pp. 616- 620, No. 5, may 1995.	

Examiner  
SignatureDate  
Considered

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